~~222, 231, 232)~~ is electrically connectable to a channel ~~(1...k)~~ of at least one other bus line ~~(111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232)~~ using ~~a~~ the switch ~~(S_1...S_k)~~.

2. (currently amended): The device according to Claim 1, ~~characterized in that~~ wherein the multiple channels ~~(1...k)~~ of a bus line ~~(111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232)~~ are alternately electrically connectable to multiple channels ~~(1...k)~~ of another bus line ~~(111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232)~~, each channel ~~(1...k)~~ of the one bus line ~~(111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232)~~ being electrically connectable to the ~~assigned~~ channel ~~(1...k)~~ of the other bus line ~~(111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232)~~, ~~the~~ individual channels of the multiple channels ~~(1...k)~~ being connectable independently of one another.

3. (currently amended): The device according to Claim 1, ~~characterized in that~~ comprising connection bus lines ~~(15, 16, 17; 25, 26, 27)~~ ~~are provided~~ between at least a part of the programmable logic circuits ~~(11, 12, 13; 21, 22, 23)~~ for direct connection of at least a part of the programmable ~~the corresponding~~ logic circuits ~~(11, 12, 13; 21, 22, 23)~~.

4. (currently amended): The device according to Claim 1, being one of multiple receiving devices and ~~characterized in that~~ wherein the multiple receiving devices ~~(1, 2; 3,4; 5,6)~~ are connectable to one another via connection devices ~~(7A, 7B, 7C; 9A, 9B)~~, the connection devices ~~(7A, 7B, 7C; 9A, 9B)~~ having switchable bus lines.

5. (currently amended): The device according to Claim 4, ~~characterized in that~~ further comprising main connection devices ~~(7A, 7B, 7C) are provided~~, each of which connects two receiving devices ~~(1, 2; 3,4; 5,6)~~ to one another, the main connection devices ~~(7A, 7B, 7C)~~ having main connection device bus lines ~~(711, 712, 721, 722, 731, 732)~~, which connect the ~~particular~~ bus lines ~~(111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232)~~ of the two receiving devices ~~(1, 2)~~ assigned to one another to one another and the

main connection device bus lines ~~(711, 712, 721, 722, 731, 732) of a main connection device (7A, 7B, 7C)~~ being alternately electrically connectable to one another in such a way that at least one channel ~~(1...k)~~ of a main connection device bus line ~~(711, 712, 721, 722, 731, 732)~~ is electrically connectable to the channel ~~(1...k)~~ of at least one other main connection device bus line ~~(711, 712, 721, 722, 731, 732)~~.

6. (currently amended): The device according to Claim 5,

~~characterized in that~~ further comprising group connection devices ~~(9A, 9B) are provided~~, each of which connects two receiving device pairs, including two receiving devices ~~(1, 2; 3,4; 5,6)~~, connected to one another using ~~a~~ the main connection device ~~(7A, 7B, 7C)~~, to one another and a group connection device ~~(9A; 9B)~~ having group connection device bus lines ~~(911, 912, 913, 914, 915, 916)~~, which are connected to the bus lines of the ~~particular~~ receiving device pair ~~(1, 2; 3, 4; 5, 6)~~, and the group connection device bus lines ~~(911, 912, 913, 914, 915, 916) of the group connection devices (9A, 9B)~~ each being switchable in such a way that each channel ~~(1...k)~~ of each group connection device bus line ~~(911, 912, 913, 914, 915, 916) of the group connection device (9A, 9B)~~ is assigned one of a plurality of switches ~~a switch (S_1...S_k)~~ and wherein each switch of the plurality of the switches is configured to be ~~the particular switches may be~~ switched on and off independently of the other switches of the plurality of switches ~~one another~~.

7. (currently amended): The device according to Claim ~~1~~ 6,

~~characterized in that~~ wherein the receiving devices ~~(1, 2, 3, 4, 5, 6)~~, the main connection devices ~~(7A, 7B, 7C)~~, and the group connection devices ~~(9A, 9B)~~ have circuit boards ~~(10, 20, 30, 40, 50, 60; 70A, 70B, 70C; 90A, 90B)~~, which are provided on their upper side and on their lower side with plug connector arrangements ~~(V_O, V_U)~~ which include multiple plug connectors situated in the same position on the ~~particular~~ circuit boards ~~(10, 20, 30, 40, 50, 60; 70A, 70B, 70C; 90A, 90B)~~ and the outward-leading bus lines of the ~~particular~~ circuit boards ~~(10, 20, 30, 40, 50, 60; 70A, 70B, 70C; 90A, 90B)~~ are electrically connected to both upper and

corresponding lower plug connectors of the ~~particular~~ plug connector arrangement ~~(V_O, V_U)~~ in the same way.

8. (currently amended): The device according to Claim 7,

~~characterized in that~~ wherein the circuit boards ~~(10, 20, 30, 40, 50, 60; 70A, 70B, 70C; 90A, 90B)~~ are positioned one over another and are mechanically and electrically connected to one another using the plug connector arrangements ~~(V_O, V_U)~~,

and wherein two circuit boards ~~(10, 20, 30, 40, 50, 60)~~ at a time of the receiving devices ~~(1, 2; 3,4; 5,6)~~ ~~being~~ are connected ~~like a sandwich~~ into a receiving device pair using a circuit board ~~(70A, 70B, 70C)~~ of a main connection device ~~(7A, 7B, 7C)~~ positioned between the two circuit boards of the receiving devices, to form a receiving-device-main-connection-device circuit board stack ~~them~~

and wherein the receiving device pair is one of several receiving device pairs and wherein the receiving device pairs ~~being~~ are connected to one another using the circuit boards ~~(90A, 90B)~~ of the group connection devices ~~(9A, 9B)~~.

9. (currently amended): The device according to Claim ~~7~~ 8,

~~characterized in that~~ wherein a spacing ~~(L)~~ is provided between some of the plug connectors of the ~~particular~~ plug connector arrangements ~~(V_O, V_U)~~, the spacing being dimensioned to allow ~~which allows~~ cool air to flow through the circuit board stack ~~sandwich~~ between the plug connectors.

10. (canceled)

11. (new) The device of Claim 1, wherein the multiple programmable logic circuits comprise FPGAs.